REMARKS

In the outstanding Office Action, the Examiner rejected claims 1-17 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent no. 6,271,056 to Farnworth et al. ("Farnworth"). Claims 1-31 remain pending in this application, with claims 1-17 presented for examination.

I. Rejection under 35 U.S.C. § 102(b)

Regarding the rejection of claims 1-17 under 35 U.S.C. § 102(b), Applicant respectfully disagrees with the Examiner's assertions and conclusions as set forth in the outstanding Office Action[1]. Accordingly, Applicant respectfully traverses the rejection on the ground that Farnworth fails to teach each and every element of the claims.

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. §102, each and every element of the claim in issue must be found, "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown in as complete detail as is contained in the . . . claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." *See* M.P.E.P. § 2131, (8th ed., 2001).

Independent claims 1, 6, and 12 recite a combination including, for example, "a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases and the interconnection base in a stacking direction." Farnworth fails to teach at least this element.

Farnworth teaches a semiconductor package including multiple semiconductor dices which are configured to provide a small outline package or multiple semiconductor

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement of characterization in the Office Action.

dices enabling high integration. In addition, Farnworth teaches producing multiple semiconductor packages simply so as to reduce production costs and to facilitate mass production. For the above objects, in the structure of Farnworth, after die 20 (see FIGS. 2A-2D, 3 and 4) is mounted on panel 10 (see FIG. 1), panel 10 is divided as a plurality of substrates 12 along boundary lines 16. Farnworth, further teaches stacked semiconductor packages 14 including two layers comprise one substrate 12 for each layer (see FIG. 2D). In FIG. 2A, reference numbers 12a, 12b and 12c refer to "a first substrate layer," "a second substrate layer" and "third substrate layer" of substrate 12, respectively. Farnworth, col. 3, line 64 - col. 4, line 5. As shown in FIGS. 2A-2D, interlevel conductors 44 are extended through *only one* substrate 12. This does not constitute a teaching of "a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases and the interconnection base in a stacking direction," as recited in independent claims 1, 6, and 12.

Moreover, Farnworth is silent regarding the interconnection structure of conductor 36, and accordingly also fails to teach the combination including, "each of the chip interconnections is formed in the same pattern, and each of the intermediate interconnections is formed in different patterns," as recited in independent claims 1, 6, and 12. Accordingly, for at least the above reasons, Farnworth fails to teach each and every element of independent claims 1, 6, and 12. Since Farnworth fails to teach each and every element of independent claims 1, 6, and 12, the reference cannot anticipate independent claims 1, 6, and 12. Accordingly, Applicant respectfully requests that the rejection of independent claims 1, 6, and 12 under 35 U.S.C. § 102(b) be withdrawn.

Claims 2-5 depend from claim 1. Claims 7-11 depend from claim 6. Claims 13-17 depend from claim 12. Since Farnworth fails to teach each and every element of independent claims 1, 6, and 12, that reference also fails to teach each and every element required by the dependent claims. Accordingly, Applicant respectfully requests that the rejection of claims 2-5, 7-11, and 13-17 under 35 U.S.C. § 102(b) be withdrawn.

Embodiments of the present application disclose, for example, multilayered semiconductor packages having a multilayered structure in which a plurality of semiconductor chips, chip mounting bases and interconnection bases are stacked in a plurality of layers. The multilayered semiconductor packages are made to improve both the chip interconnections formed on each layer of an individual chip mounting base and the wiring patterns of the intermediate interconnections formed on each layer of the individual interconnection base. This structure may increase the production efficiency in mass production of multilayered semiconductor packages, and may reduce the manufacturing cost (see Applicant's specification at, e.g., page 13, line 20 to page 18, line 17).

For example, claim 1 recites a combination including "a semiconductor device comprising a plurality of semiconductor chips having a plurality of terminals and two chip mounting bases ... stacked in two layers in a direction of thickness." In each of the chip mounting bases, "a plurality of chip interconnections electrically connected to the terminals of the mounted semiconductor chip are formed in the substantially same pattern." The semiconductor device of claim 1 further recites at least the element "one interconnection base which is interposed between the two chip mounting bases, and on which a plurality of intermediate interconnections electrically connected to each of the

chip interconnections are formed into a different pattern from a pattern the chip interconnections." Claim 1 further recites the combination including "a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases and the interconnection base in a stacking direction, and which electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases."

The semiconductor device of claim 6 differs from that of claim 1 in that "a first interconnection base" and "a second interconnection base" are employed. The "first interconnection base is interposed between the two chip mounting bases." In this "first interconnection base," "a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from a pattern of the chip interconnections." The second interconnection base "is arranged together with the first interconnection base alternately with the chip mounting bases, and on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections and the pattern of the intermediate interconnections formed on the first interconnection base."

The semiconductor device of claim 12 differs from that of claims 1 and 6 in that "a plurality of chip mounting bases" and "a plurality of interconnection bases" are employed. In the chip mounting bases, "a plurality of chip interconnections" are "electrically connected to the terminals of the semiconductor chips mounted on the chip mounting bases," and are "formed in the substantially same pattern." In the interconnection bases, "a plurality of intermediate interconnections" are "electrically

connected to the chip interconnections," and "are formed into predetermined patterns for the respective interconnection bases that are different from the pattern of the chip interconnections."

Embodiments in the specification disclose a semiconductor device wherein the chip interconnections are formed in the same pattern, and the intermediate interconnections are formed in different patterns. In this structure, signal paths comprised in the semiconductor device are switched between layers so as to prevent short-circuiting. Semiconductor chips of respective layers may be electrically connected to external interconnections by using electrically individual paths with chip interconnections and intermediate interconnections interposed.

In a conventional structure, such as shown in Figure 11, a number of chip interconnection bases tend to be needed in each of the interconnection bases. However, in the structure of the claimed invention, different patterns of chip interconnection bases need not be provided on each layer. Accordingly, as the number of chip mounting bases mounted on one interconnection base is increased, a load of managing chip mounting bases and interconnection bases is lightened. On the basis of the semiconductor device of claims 1, 6 and 12, the problems owing to board management may be solved (see, for example, "Background of the invention" and page 13, line 20 to page 18, line 17).

The semiconductor device, as recited in claims 1, 6 and 12, does not require via plugs formed individually on each chip interconnection base or interconnection bases. The semiconductor device comprises "interlevel interconnections which are formed in ... through holes extending through the chip mounting bases and the interconnection

bases [in a] stacking direction," instead of the via plugs. Owing to this, the semiconductor device may be manufactured in a simple process, and the interconnection structure of the semiconductor device is as precise as possible. The semiconductor device of claims 1, 6 and 12 solves the problems due to via plugs formed on each of the chip interconnection bases and interconnection bases.

As stated above, the semiconductor device of claims 1, 6 and 12, wherein multilayered semiconductor packages have a multilayered structure in which a plurality of semiconductor chips are stacked in a plurality of layers, may increase the production efficiency in mass production of multilayered semiconductor packages, and may reduce the manufacturing cost.

The above-mentioned structures and advantages of the semiconductor device of claims 1, 6 and 12 are supported in the specification, at for example, page 29, line 9 to page 33, line 2 and page 39, line 24 to page 41, line 10. FIGS. 9 and 10, for example, show the interconnection patterns of chip interconnection and intermediate interconnection of the semiconductor device described in claims 1, 6 and 12. For at least the above reasons, Applicant respectfully submits that claims 1-17 are not anticipated by Farnworth.

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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